IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:
Application No.:
Filed:
Title:
Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390
Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.
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770-933-9500

ASSIGNEE OF ENTIRE INTEREST
TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
8, Li-Hsin Rd. 6
Hsinchu Science Park
Hsinchu, Taiwan 300-77, R.O.C.

ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: Nov 19, 2004

Lynn Hsiao for
Chien-Wei (Chris) Chou
Director - Intellectual Property Division

Attachment A

No.	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1.	10/002,986	2001-0376	Contact hole printing by packing and unpacking	11/30/01	012354/0997
2.	10/437,374	2001-1014B	Method to improve the coupling ratio of top gate to floating gate in flash	05/13/03	Recorded 013218/0246 at the parent application USP 6,579,761
3.	10/602,229	2002-0695	Novel dual bit split gate flash memory	06/24/03	014228/0451
4.	10/411,346	2002-0536	Method of forming a metal-insulator-metal capacitor structure in a copper damascene process sequence	04/10/03	013982/0072
5.	09/310,256	1998-0574	Method to reduce particle level for dry-etch	05/12/99	009960/0894
6.	10/119,327	1998-0241BC	Method to increase coupling ratio of source to floating gate in split-gate flash	04/09/02	Recorded 009928/0175 at the parent application USP6,159,801
7.	09/249,254	1998-0275	Method of making a metal-insulator-metal capacitor in the CMOS process	02/12/99	9768/0876
8.	09/247,974	1998-0518	Key-hole free process for high aspect ratio gap filling with reentrant spacer	02/11/99	9766/0859
9.	10/099,029	2001-0701	Cleaning process for phase shift masks	03/15/02	012713/0794
10.	10/823,148	1999-0014B	Novel multi-level (4state/2-bit) stacked gate flash memory cell	04/13/04	Recorded 013501/0898 at the parent application USP6,734,055
11.	10/706,382	1999-0431	Novel method to reduce the fluorine contamination on the Al/Al-Cu pad by a post high cathod temperature plasma treatment	11/12/03	014700/0353
12.	09/783,381	2000-0171	Virtual customs broker by business-to business electronic commerce link	02/15/01	011600/0778
13.	10/410,123	2000-0526	Novel exposure method for the contact hole	04/09/03	013959/0569
14.	10/786,798	2003-0294	Space process to prevent the reverse tunneling in split gate flash	02/25/04	015032/0533
15.	10/623,907	2000-0299C	High fMAX deep submicron MOSFET	07/18/03	Recorded 012111/0905 at the parent application USP6,613,623
16.	10/443,359	2002-0162	Water soluble negative tone photoresist	05/22/03	014109/0454

Date: Nov. 19, 2004

Chien-Wei (Chris) Chou
Director - Intellectual Property Division

CERTIFICATE OF MAILING

I hereby certify that the below listed items are being deposited with the U.S. Postal Service as first class mail in an envelope addressed to:

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

on 12-02-04.

Evelyn Sanders
Evelyn Sanders

In Re Application of:

Yen-Shih Ho et al.

Serial No.: 09/249,254

Filed: 02/12/1999

Confirmation No.: 9731

Group Art Unit: 2812

Examiner: Unassigned

Docket No.: 252016-2300

For: **METHOD OF MAKING A METAL-INSULATOR-METAL CAPACITOR IN THE CMOS PROCESS**

The following is a list of documents enclosed:

Return Postcard
Certificate Under 37 CFR 3.73(b)
Power of Attorney by Assignee of Entire Interest

Further, the Commissioner is authorized to charge Deposit Account No. 20-0778 for any additional fees required. The Commissioner is requested to credit any excess fee paid to Deposit Account No. 20-0778.